1. (Four Times Amended) A method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming around vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

3. The method of claim 1, wherein the thickness of the floating gate is between approximately 500Å and 2000 Å, and the thickness of the insulator layer, when deposited, is between approximately 1000 Å and 5000 Å.

4. The method of claim 1, wherein polishing the insulator layer includes chemical mechanical polishing.

5. The method of claim 1, further comprising:

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

6. The method of claim 5, wherein depositing the dielectric layer includes depositing an ONO layer.

7. (Five Times Amended) A method of making a flash memory cell having a substrate and a tunnel oxide layer formed on the substrate, the method comprising:

depositing a floating gate layer on the tunnel oxide layer to a first thickness;

etching the floating gate layer, to provide a floating gate;

depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate such that the insulator layer has a thickness that is greater than the first thickness, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process;

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polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

9. The method of claim 7, wherein the first thickness is between approximately 500 Å and 2000 Å, and the thickness of the insulator layer, when deposited, is between approximately 1000 Å and 5000 Å.

10. The method of claim 7, wherein polishing the insulator layer includes chemical mechanical polishing.

11. The method of claim 7, further comprising:

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

12. The method of claim 11, wherein depositing the dielectric layer includes depositing an ONO layer.

14. The method of claim 7, wherein depositing the floating gate layer includes depositing a doped polysilicon.

15. The method of claim 7, wherein depositing the floating gate layer includes depositing a doped amorphous silicon.

21. (Cancelled)

22. (Cancelled)

23. (Twice Amended) A method of making a flash memory cell including a substrate, a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

depositing an insulator layer of high quality oxide on the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer of high quality oxide formed on the vertical surfaces around the floating gate to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by a LPCVD process;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

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depositing a dielectric layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.

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